Power Management in Ultra-Low Power Systems

PhD Proposal

03/01/2016

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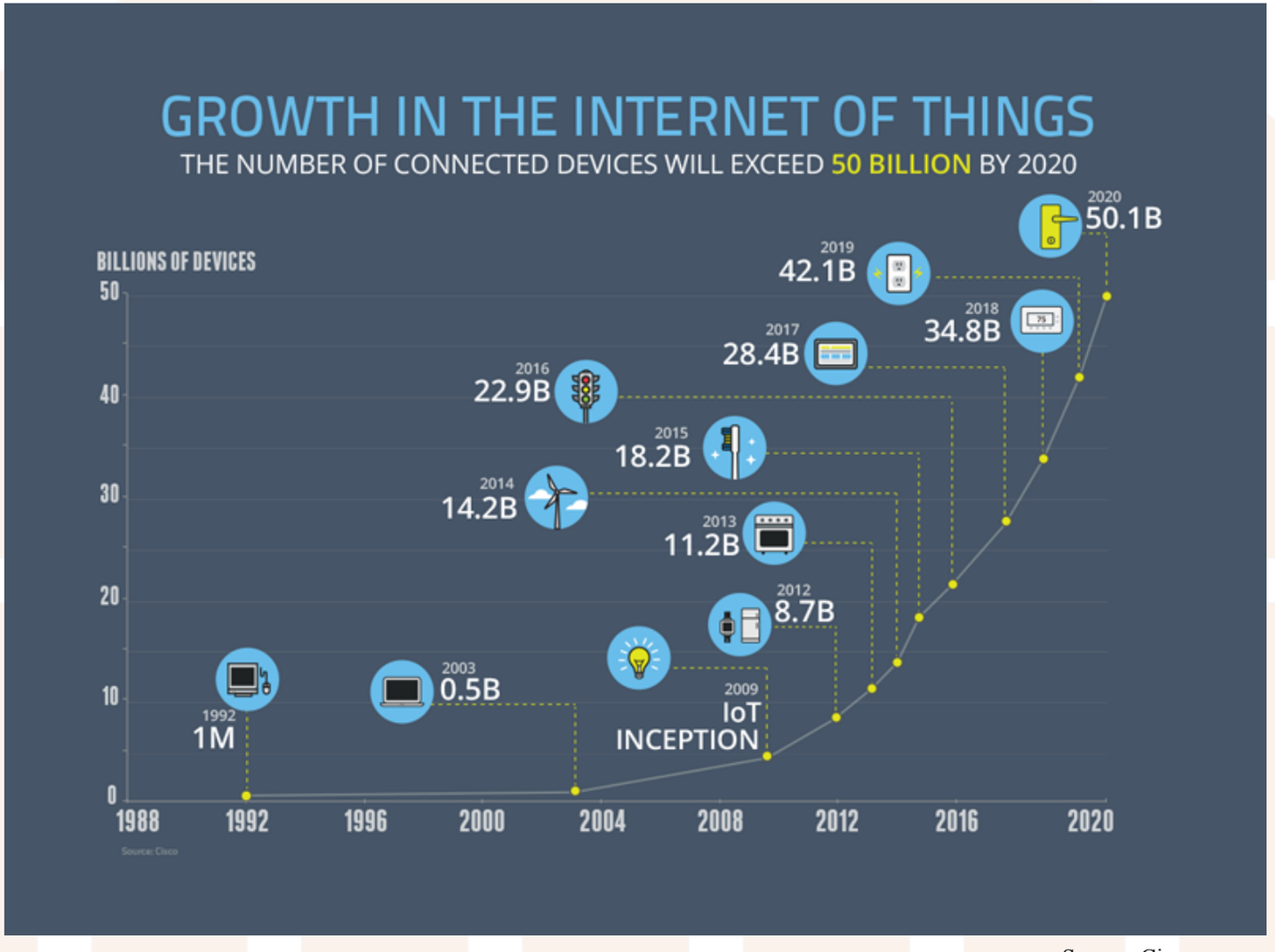
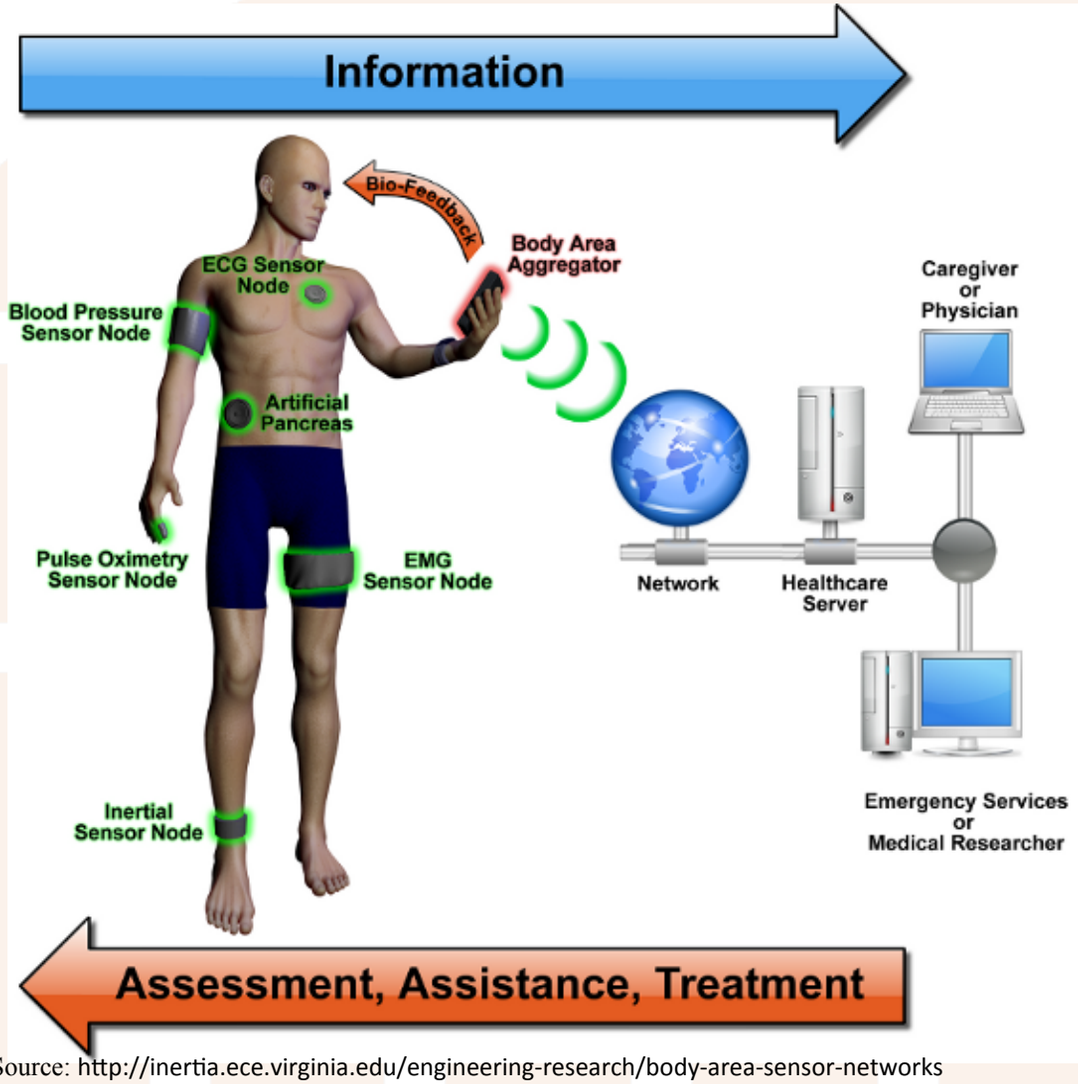
Robust
Low
Power
VLSI

Motivation



Source: Cisco

Motivation for Ultra-low Power (ULP) systems

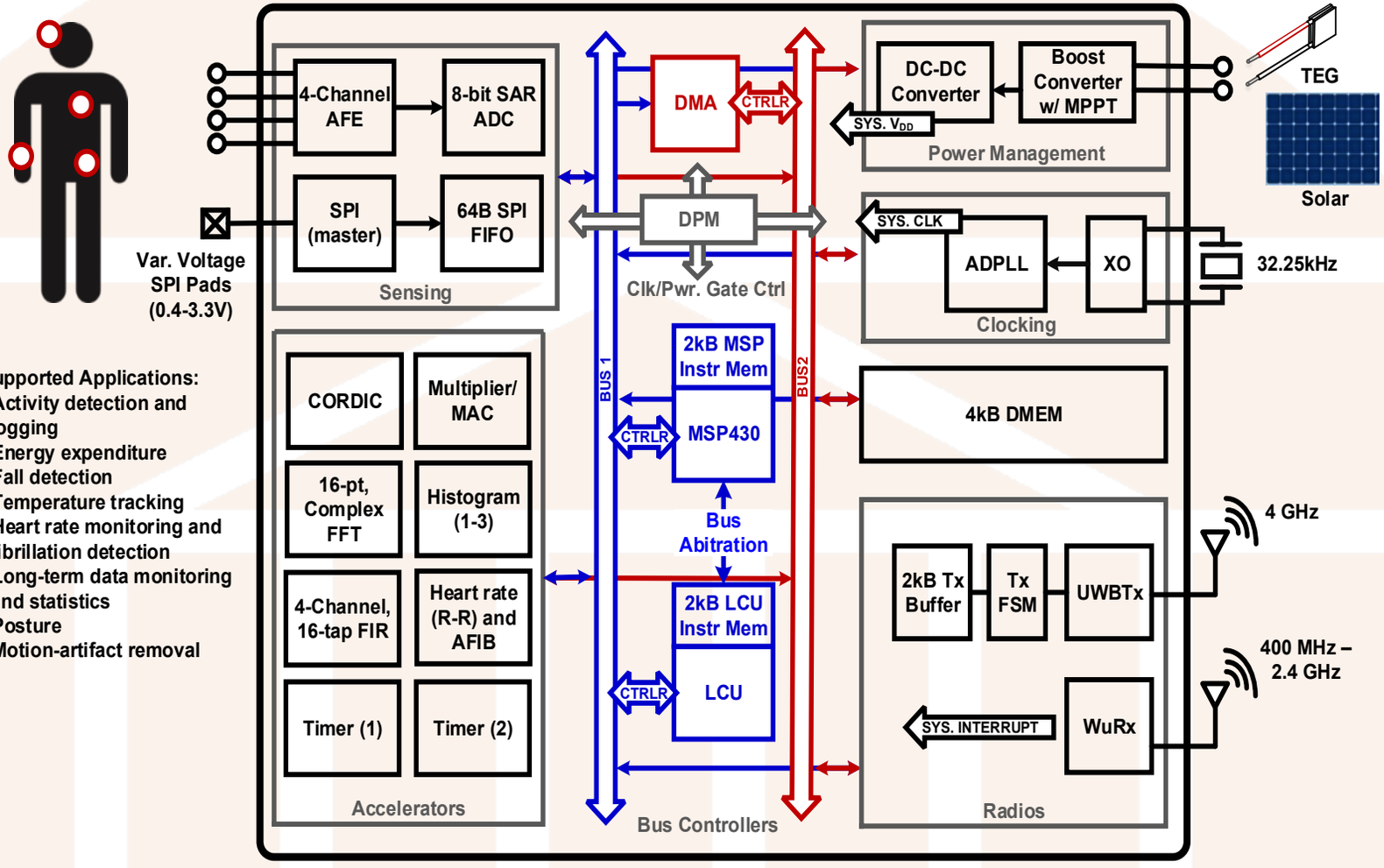


Source: http://inertia.ece.virginia.edu/engineering-research/body-area-sensor-networks

- System integration
- Small form-factors
- Longer operational lifetime for ubiquitous deployment

=>Need for Energy Harvesting and Power Management System

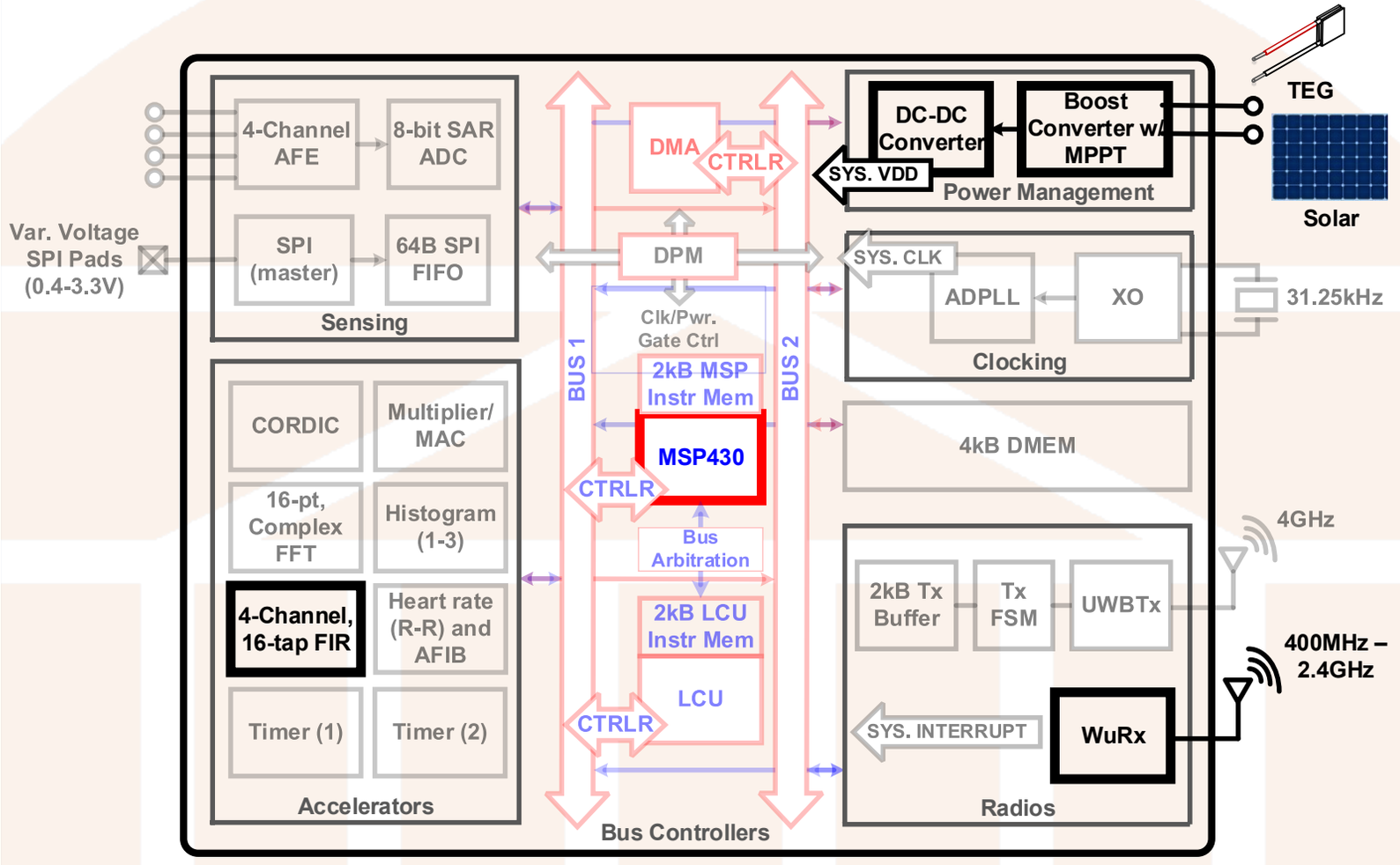
Block Diagram of a BSN SoC



Supported Applications:
- Activity detection and logging
- Energy expenditure
- Fall detection
- Temperature tracking
- Heart rate monitoring and fibrillation detection
- Long-term data monitoring and statistics
- Posture
- Motion-artifact removal

Source: Klinefelter et al. ISSCC 2015

Proposed Contributions



Source: Klinefelter et al. ISSCC 2015

Thesis Statement(s)

By employing the following features in the power management infrastructure of an IoT SoC:

- Fully integrated **energy harvesting** from multiple energy sources
- Fully integrated power-efficient **supply voltage regulation**
- Controlling **power supply variation**
- ULP digital/mixed-signal **circuit components**

Significant advantages at the system-level such as:

- Energy-autonomy and near-perpetual system operation
- A longer operational lifetime
- Smaller overall form-factor
- System flexibility and use in a wide range of applications

Outline

- Energy Harvesting
- Supply voltage regulation
- Monitoring Power supply variation
- Ultra-low-power analog/digital circuit components
- Timeline and Publications

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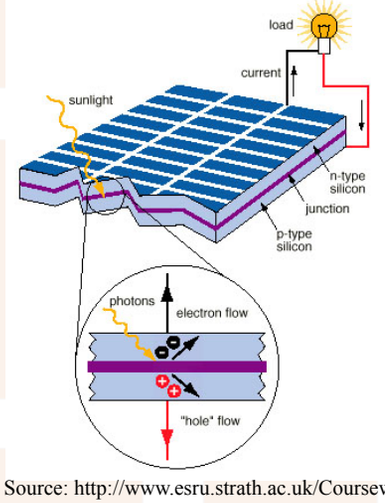
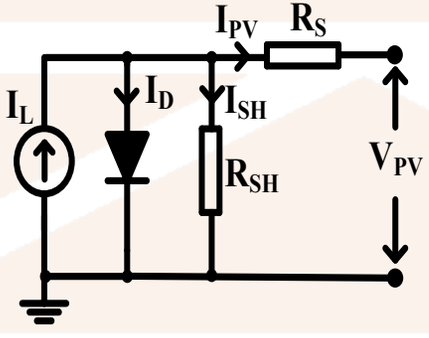
Energy Harvesting: Background

- Circuits which:
  - Extracts energy from ambient sources such as:
    - Thermal energy
    - Photovoltaic
  - Stores energy on a storage device such as a supercapacitor or
  - Uses the energy to charge a battery

Sources of Ambient Energy

Photovoltaic

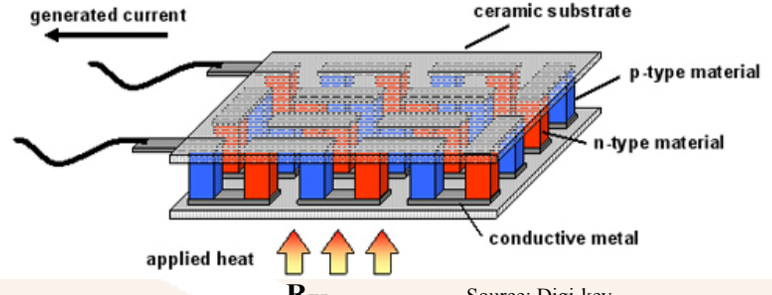




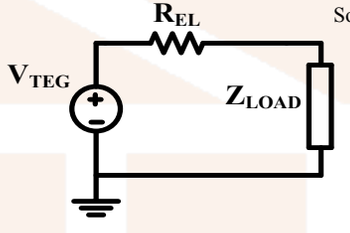
Source: http://www.esru.strath.ac.uk/Courseware/Class-16110/Images/pv1.jpg

- Photoelectric Effect
- **$I_L \propto$ Light Intensity**

Thermal



Source: Digi-key



- Seebeck Effect
- **$V_{TEG} \propto \Delta T$**

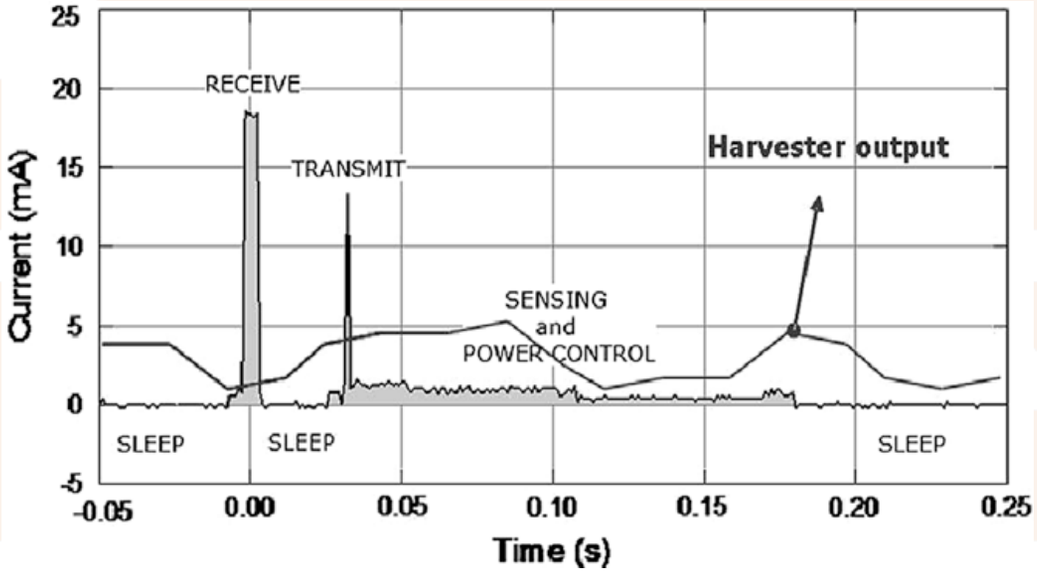
Sources of Ambient Energy

Source	Power Density	Characteristics
Ambient Light		
Indoor	**100 µW/cm^2**	Illumination from artificial light
Outdoor	**10 mW/cm^2**	Natural sunlight
Thermal Energy		
Human	**100 µW/cm^2@ 5°C gradient**	Thermal gradient between body heat and ambient
Industrial	**3.5 mW/cm^2@ 35°C gradient**	Thermal gradient between machine heat and ambient

Source: Adapted from Tan and Panda, IEEE Transactions on Industrial Electronics, 2011

=> **Extremely low available power** for harvesting in case of indoor applications and wearables

Need for Energy Storage



Source: Vullers et al., "Micropower energy harvesting", Journal of solid state electronics, 2009

Source	Battery		Supercapacitor
	Li-ion	Thin film	
Operating Voltage (V)	3-3.7	3.7	1.25
Energy Density (W h/l)	**435**	**< 50**	**6**
Self-discharge rate (%/month) at 20°C	0.1-1	0.1-1	100
Cycle life (cycles)	**2000**	**> 1000**	**> 10,000**
Temperature range (°C)	-20/50	-20/70	-40/65

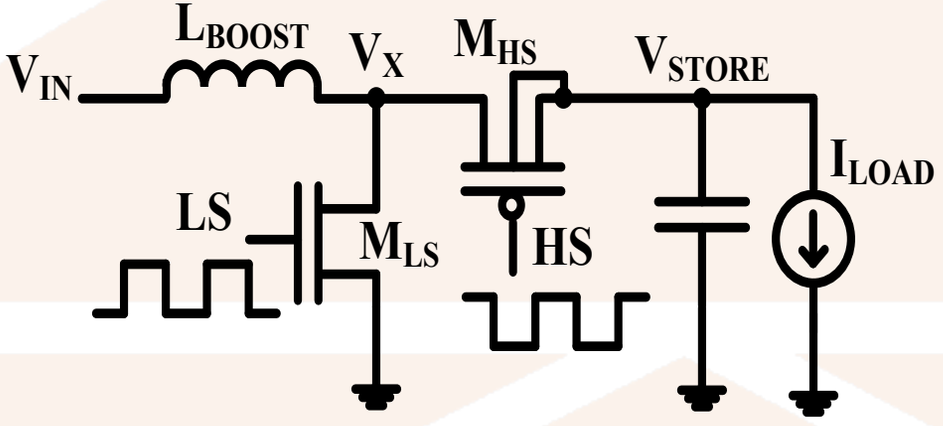
=> **Energy storage** is **necessary** to meet peak current demands of the system

=> **Battery** provides **higher energy density**, a **supercapacitor** provides greater **charge-discharge cycles**

Energy Harvesting: Background

- Types of energy harvesting architectures:
  - Inductor-based
  - Charge pumps or Switched-capacitor based
- Control Scheme consists of:
  - Maximum Power Point Tracking (MPPT)
  - Low-voltage start-up scheme
  - Powertrain-specific components such as:
    - ULP comparators for peak-inductor current control and zero crossing detection
    - Non-overlapping clock generators, level shifters
    - Digital Logic

Inductor-based Boost Converters



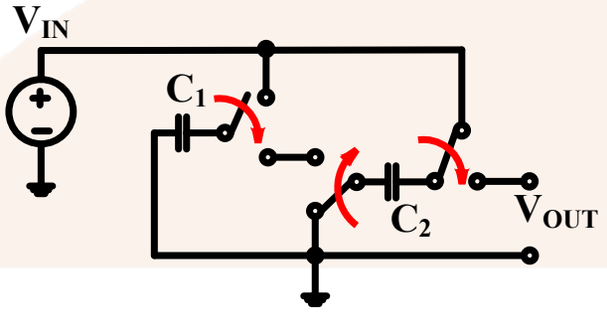
$$\frac{V_{STORE}}{V_{IN}} = 1 + \frac{T_{LS}}{T_{HS}}$$

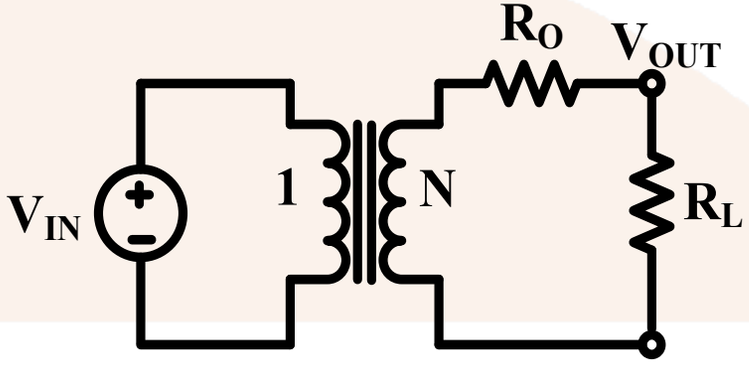
$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{V_{STORE} I_{CAP}}{V_{IN} I_{IN}}$$

Factors impacting η

- Conduction loss in the inductor (parasitic DCR), M_{HS} and M_{LS}
- Switching loss due to turning ON/OFF M_{HS} and M_{LS} ; gate-control circuits
- Leakage in M_{HS} and M_{LS}; control circuits

Switched-capacitor based Boost Converters



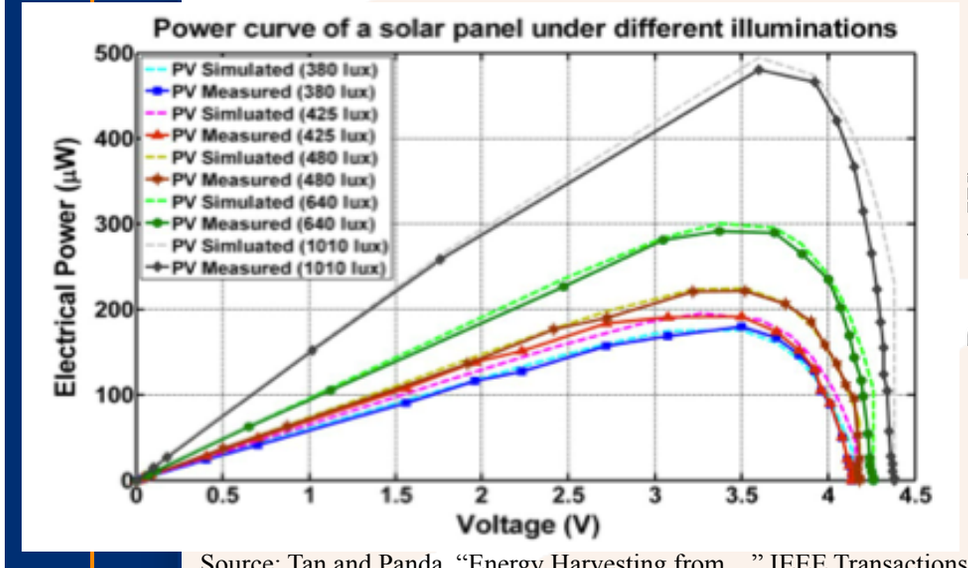


Factors impacting η

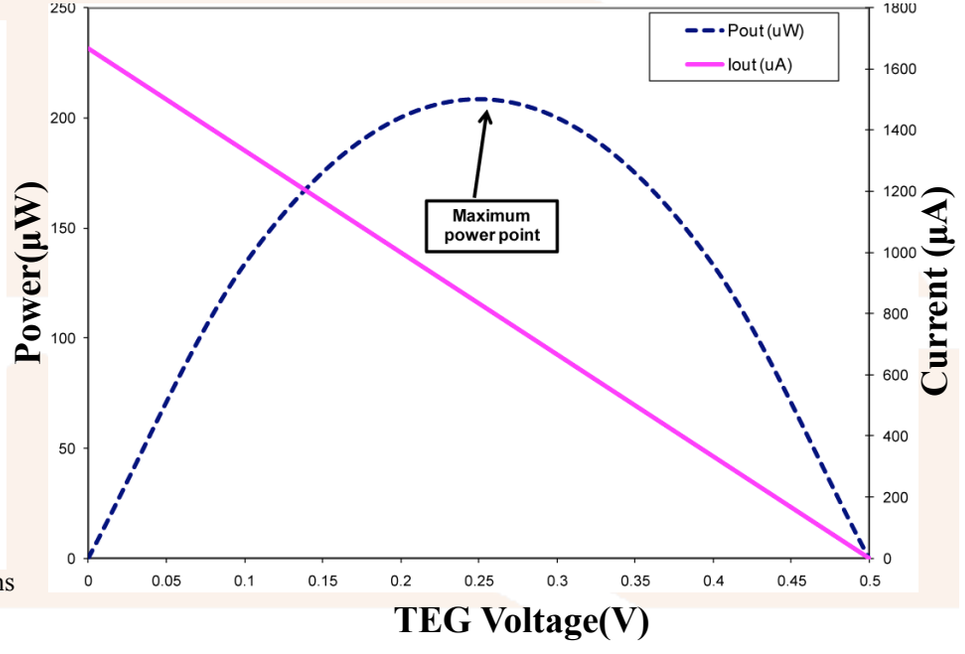
$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT} I_{OUT}}{V_{IN} I_{IN}}$$

- Topology
- Conduction loss in the switches and transfer capacitors
- Bottom plate parasitic capacitance
- Switching loss due to turning ON/OFF switches ; gate control circuits
- Contention currents in switch control, level shifters; leakage in switches

Maximum Power Point Tracking (MPPT)



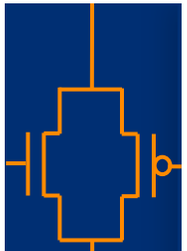
Source: Tan and Panda, "Energy Harvesting from…" IEEE Transactions on Industrial Electronics, 2011



Source: Kadirvel et al. "Power Management Functions for energy harvesting", EETimes 2012

⇒ MPP of solar and TEG are different fractions of open-circuit voltage

⇒ MPP of solar cell changes with light intensity



Low Voltage Start-up

Low output voltage from TEGs and indoor solar cells due to:

- Smaller size; Constrained form factors
- Limited temperature differential, Light intensity

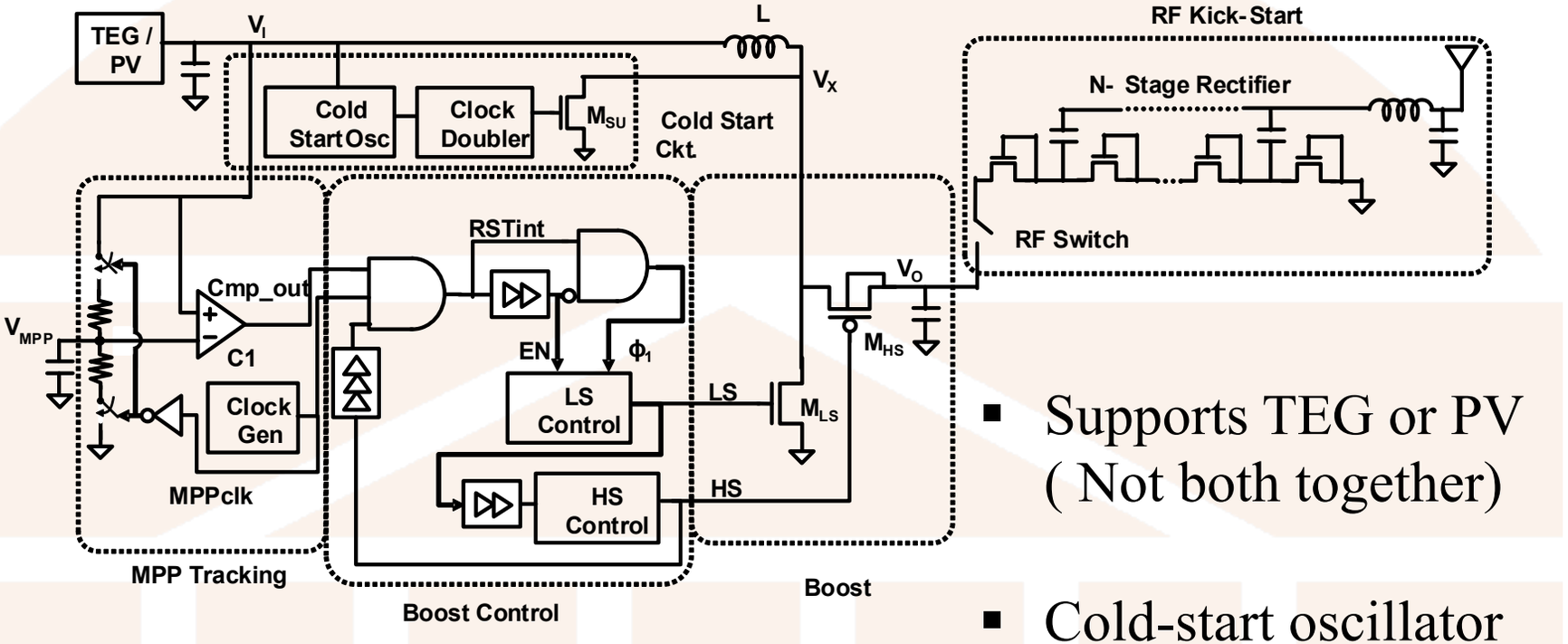
=> Low output voltage from TEG/solar cell

- Self-Powered system =>No secondary power source

⇒ **Need a low-voltage startup circuit to begin energy-harvesting.**

⇒ **Efficiency is not critical at startup**

Energy Harvesting: Prior Work



⇒ **External passives**

⇒ At a time only TEG or PV.
Configure V_{MPP} externally

- Supports TEG or PV (Not both together)
- Cold-start oscillator and RF kickstart
- Fractional o.c. MPPT

Source: Shrivastava et al. JSSC 2015

Energy Harvesting: Problem Statement and Hypothesis

Problem Statement:

Battery-less ULP systems, which harvest from a single source of energy have the following limitations :

- Less flexibility
- Less reliability and high risk from complete loss of harvested energy
- Limited operational lifetime.

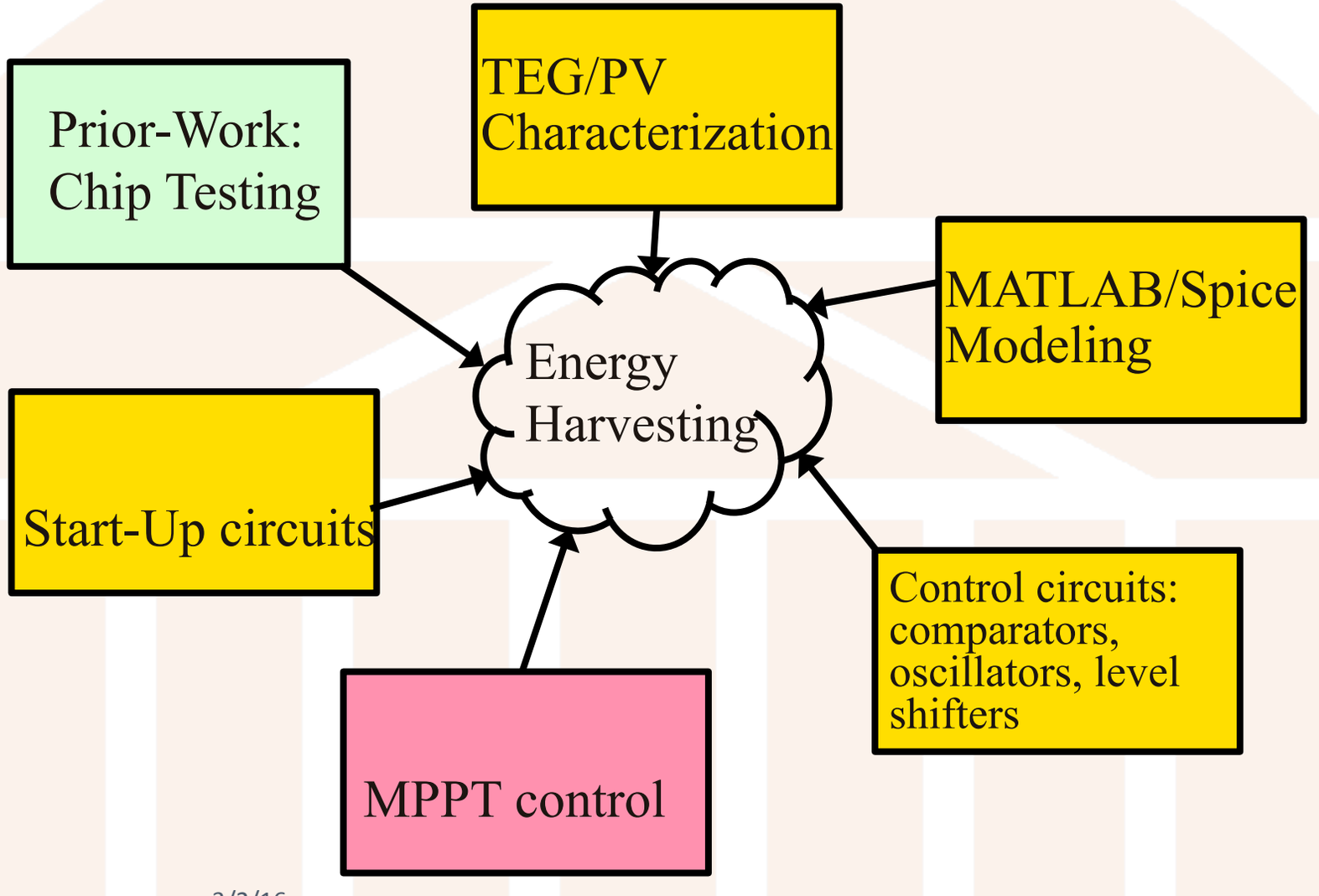
Hypothesis:

By enabling the system to harvest from multiple energy sources, the system can operate reliably over long intervals of time and with changing environmental scenarios, making the system more flexible and fit into a wide range of self-powered applications

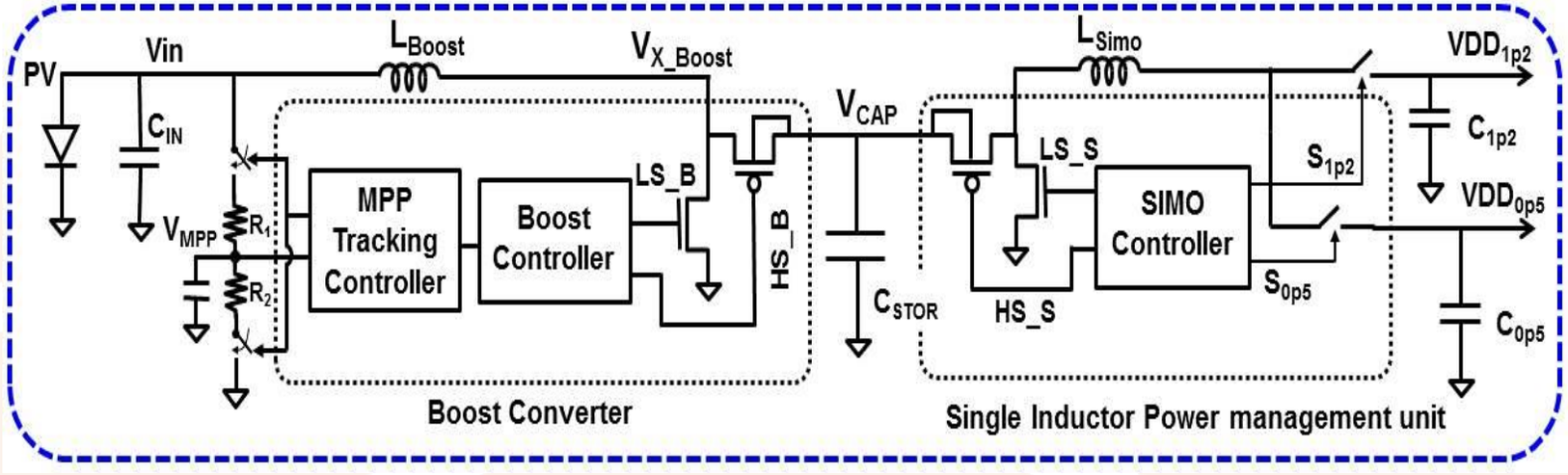
Energy Harvesting: Research Questions

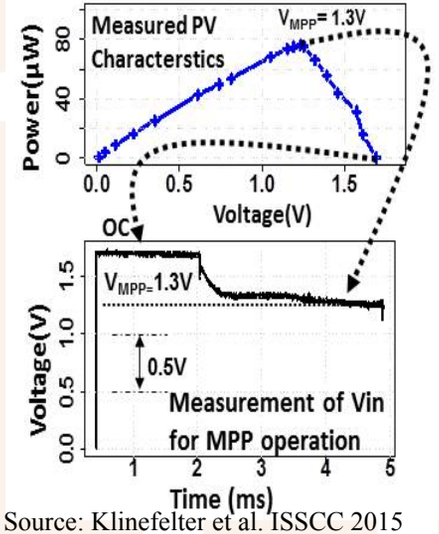
- What kind of powertrain topology would enable the flexibility to harvest from both TEG and indoor solar
- What approach needs to be taken for MPPT in a multi-modal harvesting environment
- What kind of start-up schemes would work best in a multi-modal Energy Harvesting-Power Management Unit (EH-PMU)

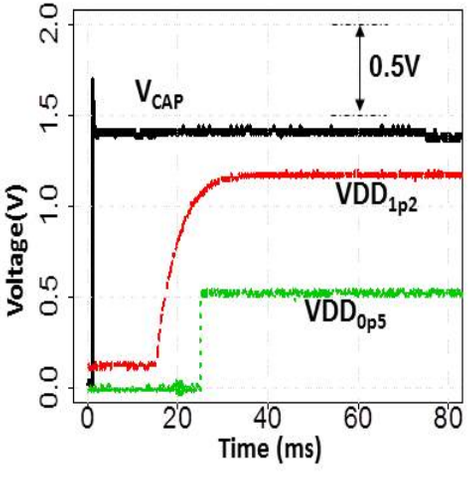
Approach


Prior-Work:
Chip Testing
TEG/PV
Characterization
MATLAB/Spice
Modeling
Energy
Harvesting
Start-Up circuits
Control circuits:
comparators,
oscillators, level
shifters
MPPT control

EH-PMU Chip-Testing







- Two inductors; Fractional o.c. MPPT=>External passives
- Cold-start at 220mV
- Sensitive to PCB layout; lacks controllability and observability

Source: Klinefelter et al. ISSCC 2015
Source: Roy et al. IEEE TBioCAS 2015

Energy Harvesting: Figures of Merit

- Efficiency
- Minimum input voltage
- Output Voltage
- Area

Energy Harvesting: Contributions

- A first–order model, for design space exploration for powertrain topologies.
- A hybrid MPPT control to achieve peak power efficiency for both solar and thermal energy harvesting
- A start-up circuit/architecture for enabling low-voltage system startup.
- A fully-integrated energy harvesting platform for thermal and solar energy harvesting with low-voltage startup and MPPT

Outline

- Energy Harvesting
- Supply voltage regulation
- Monitoring Power supply variation
- Ultra-low-power analog/digital circuit components
- Timeline and Publications

Supply Voltage Regulation: Background

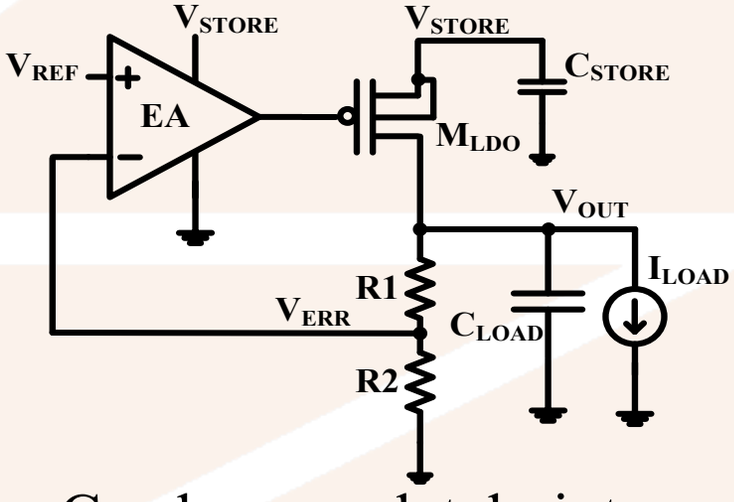
- A class of power delivery circuits which:
  - Provides stable, well regulated supply voltages to different components of an SoC
  - Delivers power to the SoC components across different operating modes with maximum efficiency
  - Can be off-chip (PMIC) or on-chip (Integrated Voltage Regulators or IVRs)

=> IVRs are more suitable for systems with constrained form factors

Supply Voltage Regulation: Background

- Types of Voltage Regulators
  - Linear Regulators such as Low-Drop-Out (LDO)
  - Switching Regulators:
    - Inductor-based Buck converter
    - Switched-Capacitor-based Buck converters

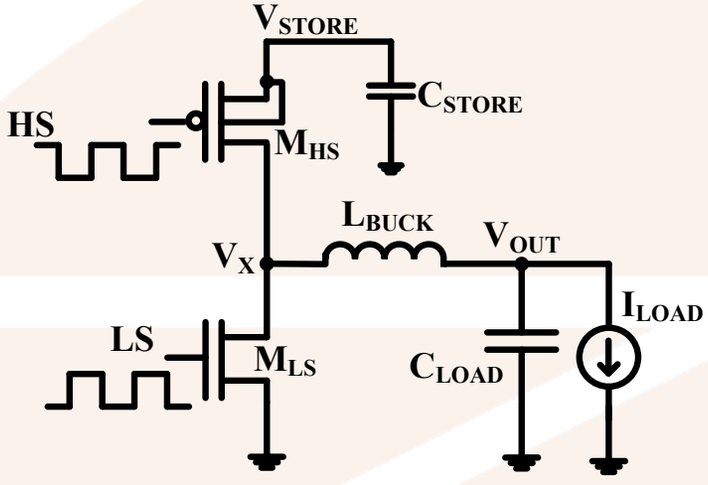
Supply Voltage Regulation: LDOs



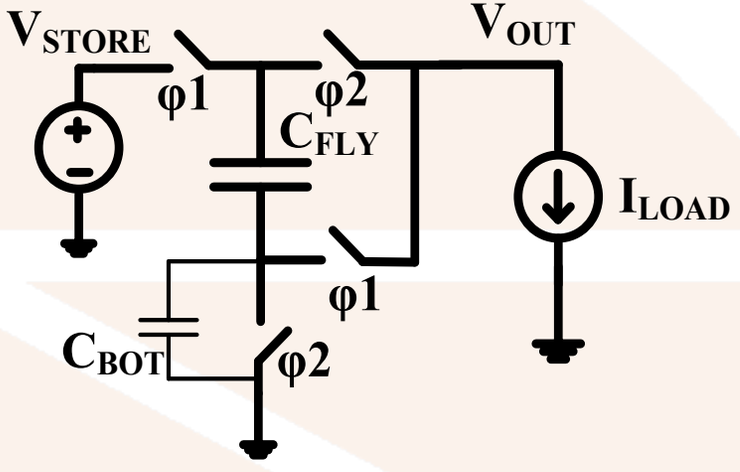
$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT} I_{LOAD}}{V_{STORE}(I_{LOAD} + I_{CONTROL})}$$

- Can be completely integrated. -> **No off-chip passives**
- No switching noise => good **filter**
- Can **step-down** but **not step-up. Hence $V_{OUT} < V_{STORE}$**
- **Low Power-efficiency** for **high conversion ratios (V_{OUT}/V_{STORE})**

Supply Voltage Regulation: Switching Regulators



Inductor-based Buck Converter



2:1 Switched-Cap based converter

- **External passives (Inductor)** required
- **Performance** depends on **PCB layout, package parasitics.**
- Supports **wide-range** of **conversion ratios**

- **Completely integrated-> No passives**
- **Switch-dominated** or **cap-dominated**
- **Conversion ratios** depend on **topology**

Voltage References

- Provides **stable** reference voltage **ideally independent** of **supply voltage** and **temperature**

- Used in analog/mixed signal circuits such as voltage regulators, ADC's etc.

- Options:
  - Bandgap Reference: ~µW **Power**, ~1V operation
  - ΔV_T –based voltage reference: **Low** power, **sensitive** to **PVT variations**

=> Need **Low Voltage**, **Low Power voltage reference** for high power-efficiency power converters and ULP systems

Supply Regulation: Problem Statement and Hypothesis

Challenges:

- Different supply voltages, electrical specs of various circuit components.
- Achieve high efficiency
- Need for off-chip passives and components : ↑cost
  ↑form-factor
- Reliability and limited operational lifetime.

Hypothesis:

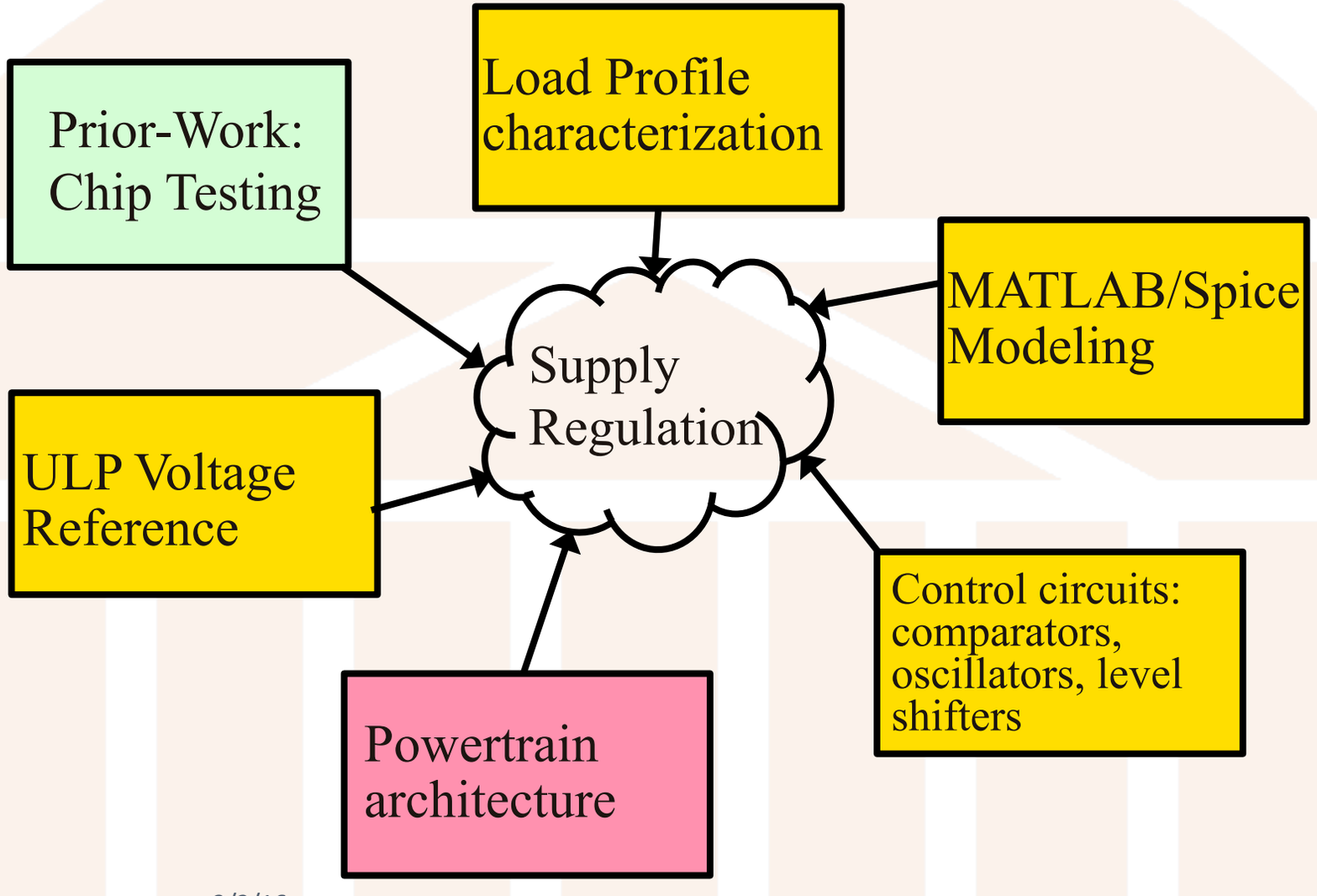
A fully-integrated and a hybrid topology (such as switched-cap + LDO) along with an adaptive supply regulation scheme can provide improvements in

- Overall power-efficiency
- Smaller form-factor and reduced design complexity

Supply Regulation: Research Questions

- Single-stage or cascaded topology?
- How much ripple or power supply variation can be tolerated?
- Trade-offs between strong line regulation vs. power-efficiency?
- Sensitivity of a voltage reference circuit? How much tolerance to power supply variation and temperature?

Approach


Prior-Work:
Chip Testing
Load Profile
characterization
MATLAB/Spice
Modeling
Supply
Regulation
ULP Voltage
Reference
Control circuits:
comparators,
oscillators, level
shifters
Powertrain
architecture

Supply Regulation: Figures of Merit

- Efficiency
- Ripple
- Minimum Input Voltage
- Maximum load current
- Response time
- Area

Supply Regulation: Contributions

- An architecture for supply-regulation targeted at achieving high power efficiency at 1-10μW load comparable or better than the state-of-the-art
- A ULP voltage reference circuit operating at low supply voltage and suitable for light-load regulation.
- A framework or model for evaluating ripple and supply voltage variation vs. efficiency

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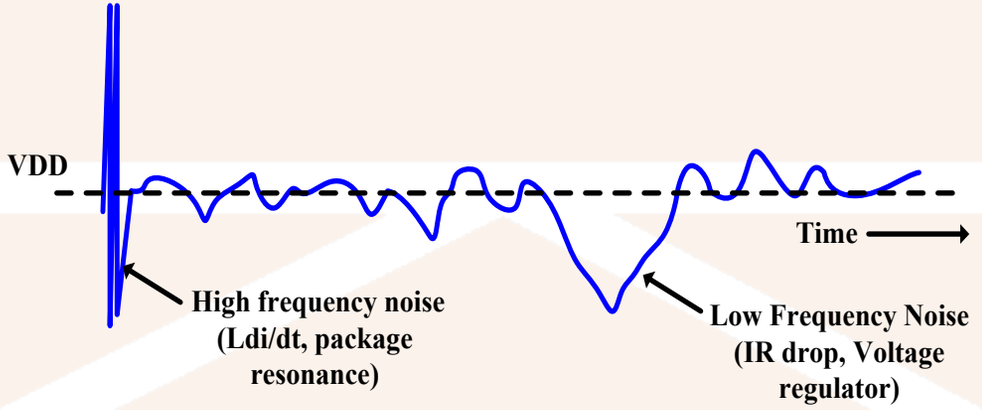
- Monitoring Power supply variation
- Ultra-low-power analog/digital circuit components
- Timeline and Publications

Power Supply Variation: Background



Adapted from: Muhtaroglu, A.; et al. "On-die droop detector for analog sensing of power supply noise," , JSSC 2004

- High Frequency: $L\frac{di}{dt}$, package resonance
- **Low Frequency: Voltage Regulator, IR drop**

Power Supply Droop Monitors: Prior Work

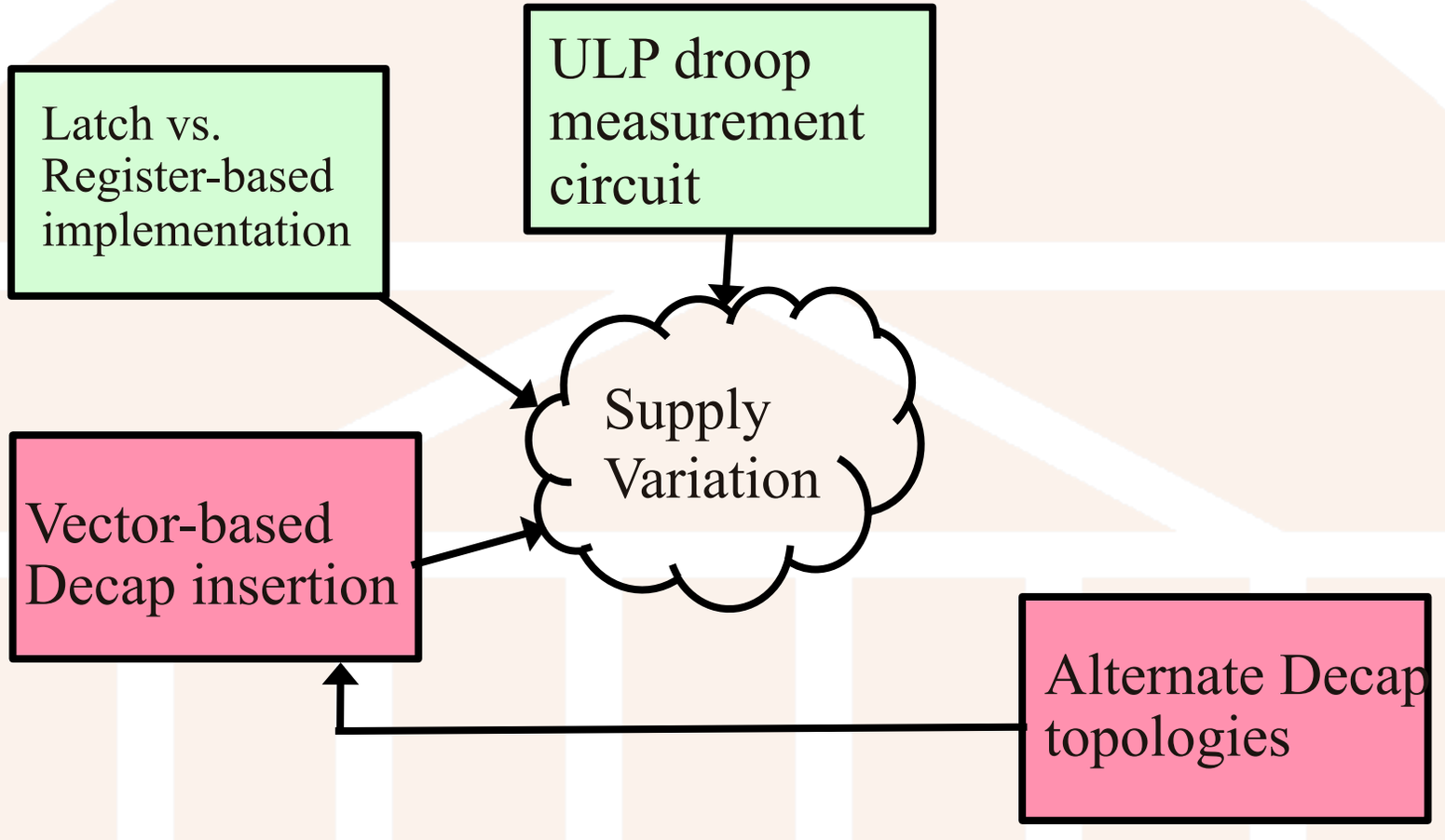
- On-Die Analog Droop detectors ➔Higher Quiescent currents
- Adaptive clock distribution and in-situ timing error detection and correction➔Area
- Decoupling capacitors ➔Gate leakage

=> Need **low cost**, **compact, ULP** supply voltage **droop monitors** in **high-efficiency** voltage regulators for ULP systems

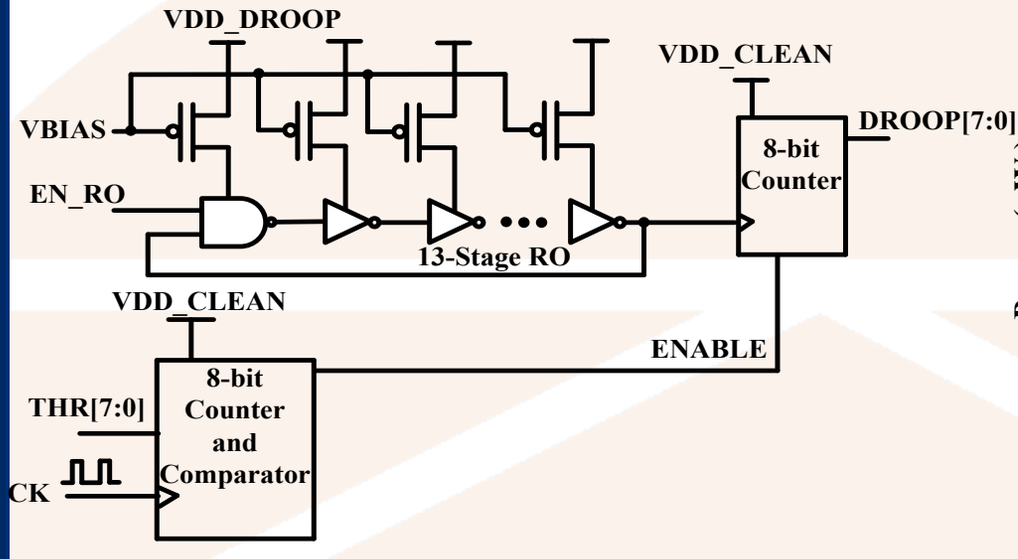
Power Supply Variation: Research Questions

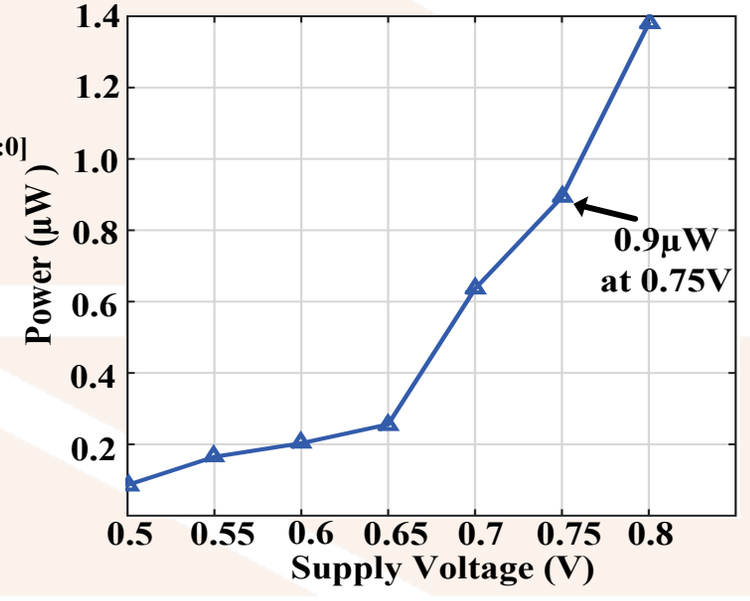
- What architectural methods/circuit techniques/design methodologies provide better power supply noise immunity?
- What bandwidth should an on-die power supply noise detector support?
- How much resolution is acceptable?
- What will be the calibration scheme for measuring power supply noise?

Approach


ULP droop measurement circuit
Latch vs. Register-based implementation
Supply Variation
Vector-based Decap insertion
Alternate Decap topologies

All-Digital Power Supply Droop Measurement Unit





Source: Roy A. et al. ISCAS 2016

- Current-controlled ring oscillator operating at noisy supply
- A counter running at noise-free supply counts RO clock cycles

Power Supply Variation: Figures of Merit

- Power Consumption
- Resolution for droop measurement
- Area

Supply Voltage Variation: Contributions

- Evaluating latch-based design implementation flow for better power supply noise immunity
- Low power droop measurement scheme using digital circuits
- Design flow for vector-based dynamic IR analysis and alternate decoupling capacitor (such as active decoupling capacitors) topologies

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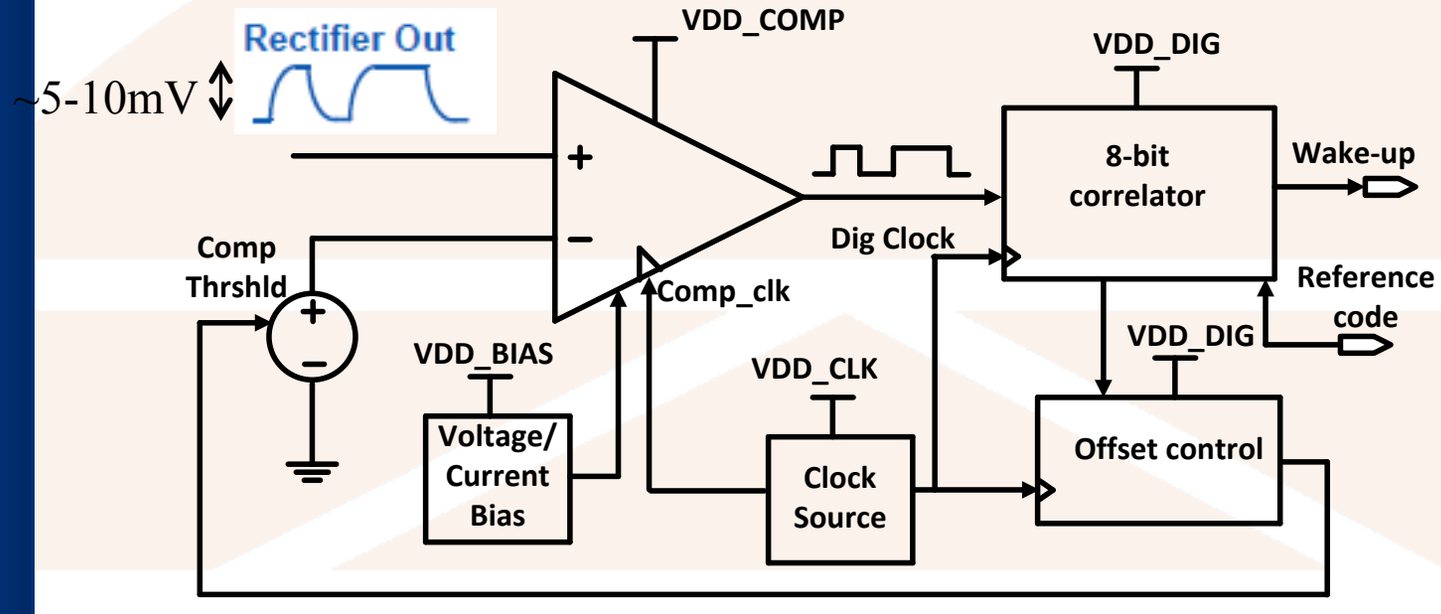
Ultra-low-power circuit components

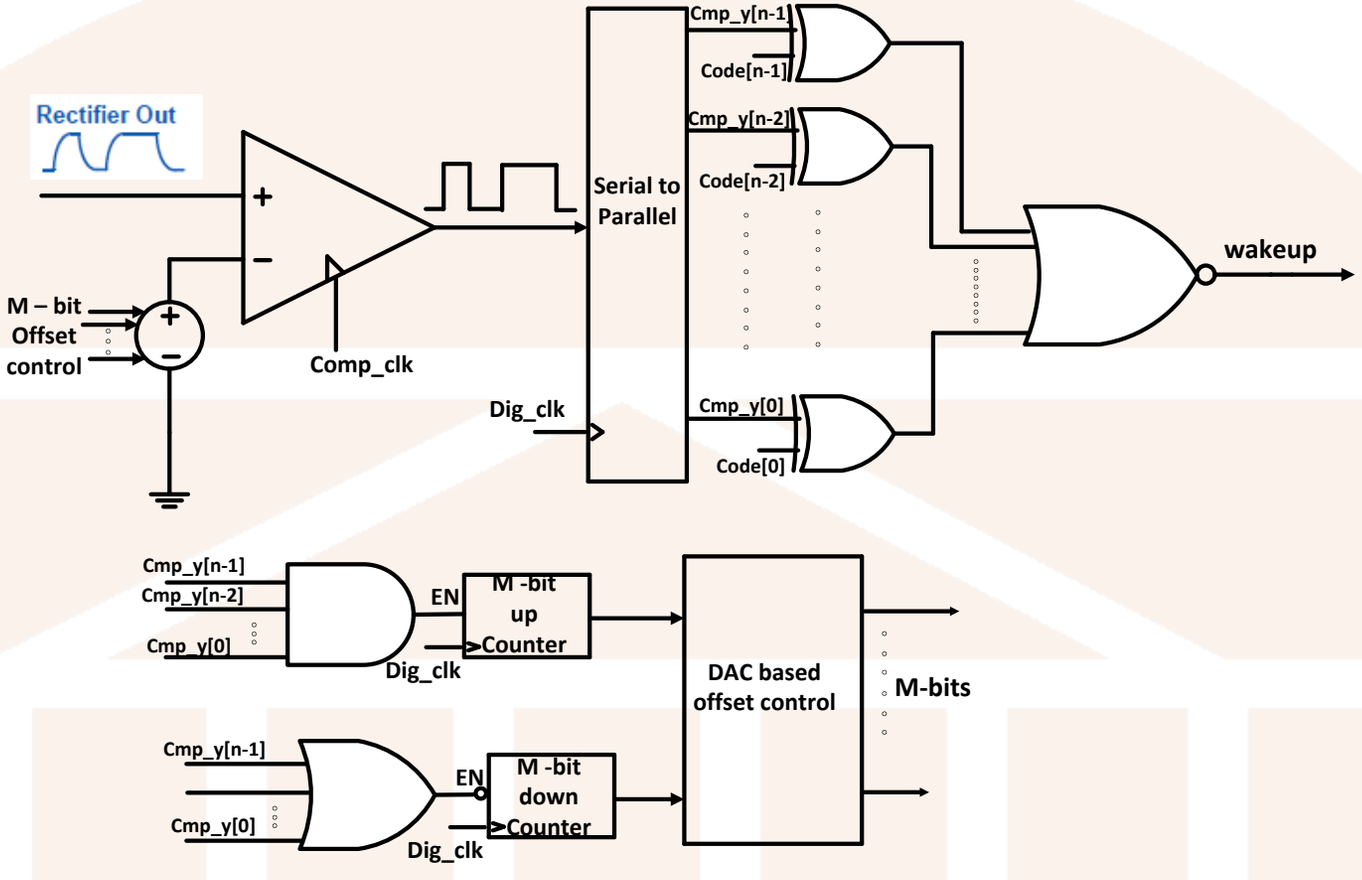
- ULP wakeup-radio system
  - Low-power, low input-referred offset comparators
  - Low-power digital correlators
- ULP Digital circuits in novel process technologies
  - MSP430 processor in MITLL 90nm FDSOI
  - A 16-bit, 32-tap FIR filter in 55nm Deeply Depleted Channel (DDC)

Ultra-low-power wake-up receiver



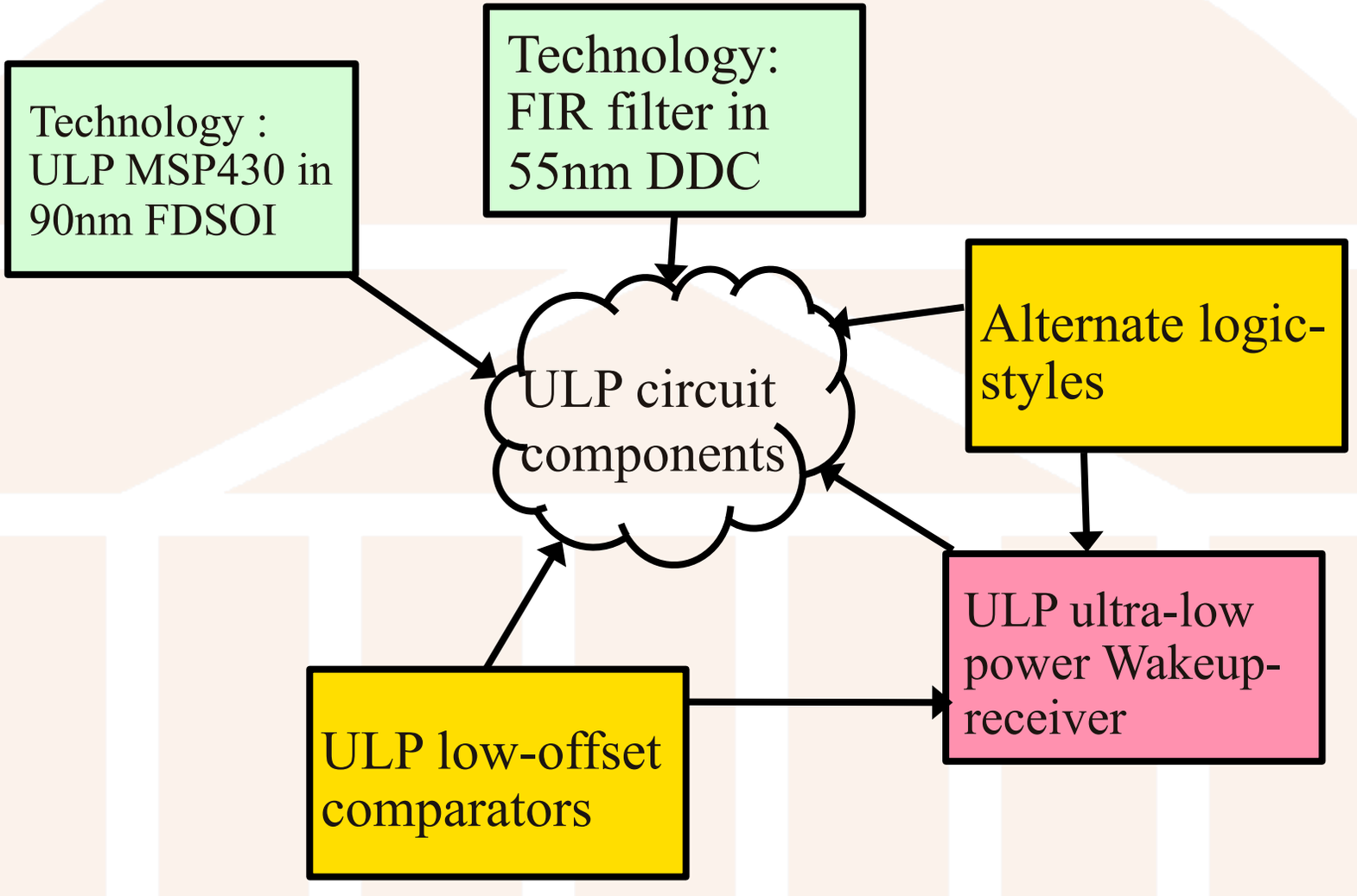
- 10nW total system power budget ➔ULP comparator, biasing, digital logic
- 5-10mV rectified output ➔ Need very **low input-offset**
- ~1V operation

ULP Processing for Wake-up



- 8-bit correlator (n=8)
- 4-bit offset control (M=4)
- Correlator + offset control consumes 3.6nW at 0.5V supply and 10kHz

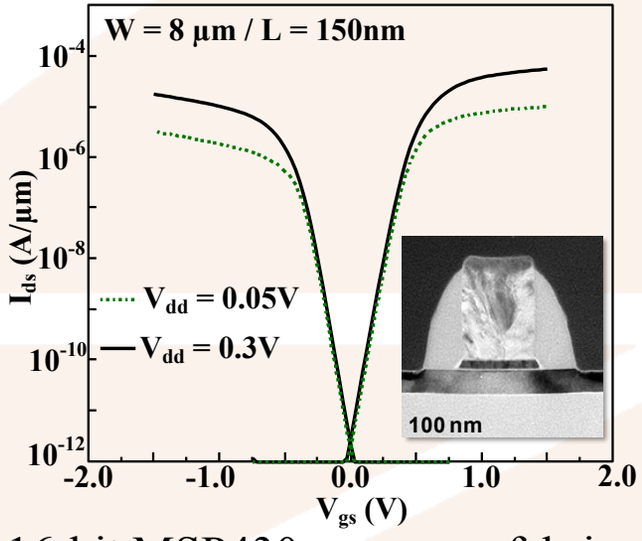
Approach

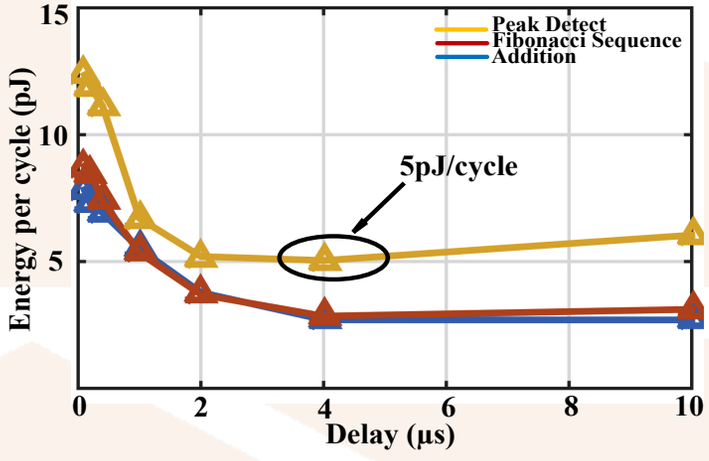

Technology :
ULP MSP430 in
90nm FDSOI
Technology:
FIR filter in
55nm DDC
ULP circuit
components
Alternate logic-
styles
ULP ultra-low
power Wakeup-
receiver
ULP low-offset
comparators

ULP comparators and digital processing: Figures of Merit

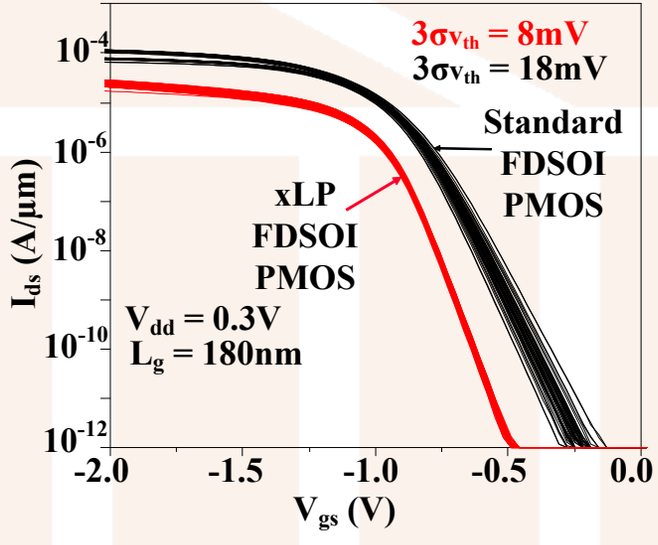
- Power Consumption
- Operating voltage and clock frequency
- Input-referred offset and noise
- Bandwidth

ULP MSP430 Processor in 90nm FDSOI process





- 16-bit MSP430 processor fabricated in 90nm FDSOI
- Process optimized for sub-V_T operation
  - Reduced V_T variation
  - Steeper sub-V_T slope, higher I_{ON}/ I_{OFF}
- Processor consumes 1.3 µW and 5pJ/ cycle at 0.4V and 250kHz



Source: Roy A. et al. ISQED 2016

Outline

- Energy Harvesting
- Supply voltage regulation
- Monitoring Power supply variation
- Ultra-low-power analog/digital circuit components
- Timeline and Publications

Research Timeline

Subject	#	Task Description	Status	Related Publications
Energy harvesting from multiple modalities	1	Architecture exploration and literature review	Completed	
	2	Testing and evaluation of previous baseline architecture	Completed	[AR1][AR2]
	3	Modeling, characterization and design space exploration of harvester topologies, MPPT, start-up	April'16	
	4	Chip tapeout with MPPT and cold-start-Phase I	May'16	
	5	Chip Testing-Phase I	Oct'16	[AR6]
	6	Chip tapeout with entire multi-modal harvesting system-Phase II	Nov'16	
	7	Chip Testing-Phase II	Mar'17	[AR7][AR10]
Voltage Regulation	1	Architecture exploration and literature review	Completed	
	2	Testing and evaluation of previous baseline architecture	Completed	[AR1][AR2]
	3	Modeling, characterization and design space exploration of converter topologies	April'16	
	4	Chip tapeout-Phase I-components	May'16	
	5	Chip Testing-Phase I	Oct'16	[AR8]
	6	Chip tapeout-Phase II-integrated system	Nov'16	
	7	Chip Testing-Phase II	Mar'17	[AR9][AR10]
Power supply variation in ULP systems	1	Architecture exploration and literature review	Completed	
	2	Exploring circuit robustness between latch vs. register based digital circuits	Completed	[AR4]
	3	All digital low-frequency droop measurement scheme	Completed	[AR4]
	4	Active decoupling circuit design	Nov'16	
	5	Methodology for dynamic IR drop analysis and decap insertion	Dec'16	[AR12]
Characterization and demonstration of ultra low-power circuit components	1	Architecture exploration and literature review	Completed	
	2	ULP Microprocessor implementation in 90nm FDSOI	Completed	[AR3]
	3	FIR filter implementation in 55nm DDC	Completed	[AR5]
	4	Design space exploration of various comparator topologies for ULP wakeup receiver	Completed	
	5	Chip tapeout for integrated wakeup-radio with ULP comparator,clocking and digital processing	May'16	
	6	Chip Testing-Wakeup-radio	Nov'16	[AR11]
Write-up		Thesis writing	April'17	

Publications

[AR1] A. Klinefelter, N.E. Roberts, Y. Shakhsheer, P. Gonzalez, A. Shrivastava, **A. Roy**, K. Craig, M. Faisal, J. Boley, Seunghyun Oh, Yanqing Zhang, D. Akella, D.D. Wentzloff, B.H. Calhoun, "21.3 A 6.45µW self-powered IoT SoC with integrated energy-harvesting power management and ULP asymmetric radios," in *Solid- State Circuits Conference - (ISSCC), 2015 IEEE International* , 22-26 Feb. 2015

[AR2] A. Roy, A. Klinefelter, F. B. Yahya, X. Chen, L.P. Gonzalez-Guerrero, C.J. Lukas, D.A. Kamakshi, J. Boley, K. Craig, M. Faisal, S. Oh, N.E. Roberts, Y. Shakhsheer, A. Shrivastava, D.P. Vasudevan, D.D. Wentzloff, B.H. Calhoun, "A 6.45 µW Self-Powered SoC With Integrated Energy-Harvesting Power Management and ULP Asymmetric Radios for Portable Biomedical Systems," in *Biomedical Circuits and Systems, IEEE Transactions on* , vol.9, no.6, pp.862-874, Dec. 2015

[AR3] A.Roy, P. Grossmann, S. Vitale, B.H. Calhoun, "A 1.3µW, 5pJ/cycle sub-threshold MSP430 processor in 90nm xLP FDSOI for energy-efficient IoT applications," in *Quality Electronic Design (ISQED), 2016 17th International Symposium on*, 15-16 March 2016

[AR4] A.Roy, B.H. Calhoun, "Exploring circuit robustness to power supply variation in low-voltage latch and register-based digital systems", in *Circuits and Systems (ISCAS), 2016 IEEE International Symposium on* , 22-25 May 2016

Anticipated Publications

[AR5] H. N. Patel, **A. Roy**, F. B. Yahya, N. Liu, K. Kumeno, M. Yasuda, A. Harada, T. Ema, B. H. Calhoun, "Ultra Low Leakage 55nm Deeply Depleted Channel Technology with Reverse Body Biasing and Subthreshold Operation to Minimize 6T SRAM and Logic Energy", Submitted to Symposium on VLSI Circuits, 2016

[AR6] MPPT control scheme and cold start circuit for enabling harvesting from multiple modalities

[AR7] Energy harvesting platform with cold-start, MPPT and battery supervisory circuit

[AR8] Voltage reference and bias circuits in ultra low power management units

[AR9] Supply regulation system at ultra-light-load currents

[AR10] Complete power management unit with integrated energy harvesting, supply regulation with MPPT, cold-start and battery supervision

[AR11] Ultra-low-power wakeup-radio system with ULP comparators and digital correlators

[AR12] Active decoupling capacitor circuit design and methodology for active and passive decap distribution for mitigating power supply droop.

High Level Impact

Achieve energy-autonomy, longer operational lifetime and reduce form factors in ULP SoCs

- Energy harvesting from multiple energy sources
- Supply regulation for delivering harvested power to various components of the system
- Control power supply variation
- Lower power consumption of different circuit components

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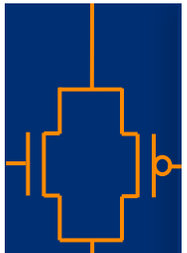
- A.Roy, P. Grossmann, S. Vitale, B. Calhoun, “A 1.3µW, 5pJ/cycle sub-threshold MSP430 processor in 90nm xLP FDSOI for energy-efficient IoT applications”, ISQED 2016



Questions ?